REMARKS

Claims 1-16 and 18-23 were pending. Claims 18-19 and 23 have been cancelled. Claims 1, 2, 9, 12 and 20-22 have been amended. Claims 24-25 have been added. Therefore, claims 1-16, 20-22, and 24-25 remain pending subsequent entry of the present amendment.

35 U.S.C. § 101 Rejections

In the present Office Action, claims 18-23 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. As claims 18-19 have been cancelled, the rejections directed to those claims are rendered moot. In addition, while Applicant does not necessarily agree with the rejections, Applicant has amended each of claims 20-22 in order to expedite prosecution of the present application. Each of claims 20-22 are believed to meet the requirements of 35 U.S.C. § 101.

35 U.S.C. § 103 Rejections

Claims 1, 2, 4, 5 and 18-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,805,918 (hereinafter "Blomgren"), in view of IAPX88 Book. As claims 18-19 have been cancelled, the rejections directed to those claims are rendered moot. Claims 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Blomgren, in view of iAPX88, and further in view of U.S. Patent No. 6,542,533 ("Bhandai") or ("Mann"). Claims 6-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Blomgren, in view of iAPX88, and in further view of U.S. Patent No. 5,887,175 ("Col"). Claims 12-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Blomgren, in view of Col and iAPX88. Finally, Applicant respectfully traverses the above rejections and requests reconsideration.

Claim 1 recites a microprocessor including "a control register that is atomically modifiable by a privileged (kernel) instruction, the control register having bit fields, the microprocessor comprising: a core, for receiving the privileged instruction and for atomically modifying the control register upon execution of the privileged instruction." In the present Office Action, it is suggested that the above highlighted features are disclosed by Blomgren. However, Applicant has reviewed the newly cited reference and submits that Blomgren does not disclose these features.

In paragraphs 7-9of the present Office Action, it is stated that:

> "Blomgren taught . . . a . . . [m]icroprocessor . . . having a control register (EFLAGS register) . . . that is atomically modifiable by a privileged (kernel instruction)[(e.g., see col. 6, lines 12-25)[The EFLAGS register has control bits that are set or cleared only by complex or infrequently used CISC instructions such as privileged instructions] . . . As to the atomically modifying the control register the control bits were modified by privileged instructions in the Blomgren system as discussed above. The status bits such as the interrupt enabled flag is a flag that was used by user mode programs to process interrupts and therefore since these bits were "seen by" the user mode programs then their modification would have been atomic (e.g., see col. 8, lines 3-7 and col. 14, lines 46-63 and col. 9, lines 39-60).

In the above, a number of portions of Blomgren are cited as ostensibly teaching the above highlighted features. However, Applicant does not find the recited features disclosed in either the above cited portions, or any of Blomgren. For example, col. 6, lines 12-25 of Blomgren merely describes complex, simpler, and emulated CISC instructions. Col. 8, lines 3-7 make no mention or suggestion of atomic modifications. The cited col. 14, lines 46-63 simply describes the use of shared registers, and how such registers may be accessed. Finally, col. 9, lines 39-60 generally describes sharing state information between programs. However, here again, there is no discussion concerning atomic modifications. Finally, Applicant does not agree with the examiner's comment that "status bits such as the interrupt enabled flag is a flag that was used by user mode

programs to process interrupts and therefore since these bits were "seen by" the user mode programs then their modification would have been atomic." Whether or not a particular status bit is "seen by" a user mode program does not necessitate that modifications to such a bit be atomic. Accordingly, these features are neither taught nor suggested by the cited art, either singly or in combination, and a prima facie case of obviousness has not been established. Therefore, claim 1 is patentably distinguished for at least these reasons. As claims 12 and 20 include similar features, these claims are similarly distinguished.

In addition to the above, claim 1 recites the additional features "wherein the control register is not accessible when the microprocessor is executing unprivileged instructions." These features correspond to prior claim 2. Paragraph 13 of the present Office Action suggests the following disclosure of Blomgren teaches the above features:

> "The dual-instruction set processor directly executes only the simpler CISC instructions. Many of these simpler CISC instructions set or clear the flag bits in Table 2. However, the control bits in Table 3 are set or cleared by complex or infrequently used CISC instructions such as privileged instructions. These instructions are therefore emulated. Only the simple CISC instructions will modify the flag bits in the CISC EFLAGS register. Emulated instructions will modify the control bits in the CISC EFLAGS register." (Blomgren, col. 6, lines 11-20).

However, this disclosure of Blomgren merely states that complex and infrequently used CISC instructions are emulated. As the control bits of Table 3 are set or (ordinarily) modified by either complex or infrequently used CISC instructions, they will be modified by emulated instructions in the dual-instruction set processor of Blomgren. However, this disclosure does not teach that the control register is not accessible when the microprocessor is executing unprivileged instructions. These features also appear in independent claims 12 and 20. Therefore, each of claims 1, 12 and 20 are believed patentably distinguished for these additional reasons as well.

Still further, each of claims 2, 24 and 25 recite the additional features wherein the control register is modified in a single cycle. These features are supported by at least paragraph 79 of the Description. Such features are wholly absent from the cited art.

Applicant believes all claims to be in condition for allowance. However, should the examiner believe otherwise, the below signed representative requests and would appreciate a telephone interview in order to facilitate a resolution.

CONCLUSION

Applicant submits the application is in condition for allowance, and notice to that effect is respectfully requested.

Respectfully submitted,
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